Abstract of the Disclosure

A delay locked loop is used in a semiconductor memory device. The delay locked loop includes a controllable delay chain block for controlling a delay time of a clock signal coupled thereto, a comparison block for detecting the increase and decrease in the delay time by comparing a reference clock signal with a delayed clock signal generated from the controllable delay chain block, and an instant locking delay control block for controlling the increase and decrease in the delay time of the delay chain block in response to an output signal of the comparison block, the delayed clock signal and the reference clock signal.